Salil Wadhavkar

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Technical Strengths and Expertise

C/C++, Python, OOP, CPU Microarchitecture, Performance Modeling, Application Analysis, Data Structures, Algorithms, Perl, Verilog HDL.

Work Experience

Qualcomm Technologies, Inc., CPU Design Center, Raleigh, NC — Raleigh, NC
CPU Performance Modeling Engineer — Jun 2013 - Present

- Develop C++ software models for various components of next-generation Qualcomm CPUs.
- Perform experiments to predict the performance of next-generation CPUs using industry standard benchmarks.
- Analyze application behavior, identify performance bottlenecks, and recommend microarchitectural solutions to improve the performance of Qualcomm CPUs.

Intel Corp., Software Services Group, Santa Clara, CA — Santa Clara, CA
Performance Tools Intern — Feb 2011 - Aug 2011

- Ported SEP, a performance profiling tool used in Intel® VTune™, to enable performance monitoring on heterogeneous processor platforms.
- Augmented the event-counting and event-sampling functionality of SEP to allow independent monitoring of different events on different processor types.
- Analyzed the performance characteristics of SPEC CPU benchmarks using SEP on different types of processors.
- Investigated parallelization of SPEC CPU benchmarks to improve performance and processor utilization on heterogeneous processor platforms.

North Carolina State University, Dept. of Electrical and Computer Engg., Raleigh, NC — Raleigh, NC
Research Assistant — Aug 2007 - Dec 2012

- Researched novel architectural techniques to improve the performance of single-threaded applications.
- Developed a microprocessor simulator in C++ that models the internal architecture of a superscalar processor.

Education

North Carolina State University — Raleigh, NC
Ph.D., Computer Engineering — Aug 2006 - Dec 2012
Thesis: Architecting a Workload-agnostic Heterogeneous Multi-core Processor
Advisor: Dr. Eric Rotenberg

Temple University — Philadelphia, PA
M.S.E., Electrical Engineering — Aug 2003 - May 2006
Thesis: Reducing the Overhead of Runahead Execution using RENO

University of Mumbai — Mumbai, India
B.E., Electronics Engineering — Sep 1999 - June 2003

Publications

A Unified View of Non-monotonic Core Selection and Application Steering in Heterogeneous Chip Multiprocessors. Sandeep Navada, Niket K. Choudhary, **Salil Wadhavkar**, and Eric Rotenberg. *Parallel Architectures and Compilation Techniques*, Oct 2013.

FabScalar: Automating Superscalar Core Design. Niket K. Choudhary, **Salil Wadhavkar**, Tanmay Shah, Hiran Mayukh, Jayneel Gandhi, Brandon Dwiel, Sandeep Navada, Hashem H. Najaf-abadi, and Eric Rotenberg. *IEEE Micro Top Picks*, Issue 3, May-Jun 2012.

FabScalar: Composing Synthesizable RTL Designs of Arbitrary Cores within a Canonical Superscalar Template. Niket K. Choudhary, **Salil Wadhavkar**, Tanmay Shah, Hiran Mayukh, Jayneel Gandhi, Brandon Dwiel, Sandeep Navada, Hashem H. Najaf-abadi, and Eric Rotenberg. *Intl. Symposium on Computer Architecture*, Jun 2011.

FabScalar. Niket K. Choudhary, **Salil Wadhavkar**, Tanmay Shah, Sandeep Navada, Hashem H. Najaf-abadi, and Eric Rotenberg. *Workshop on Architectural Research Prototyping (WARP)*, with ISCA-36, Jun 2009.

Professional Affiliations

Phi Kappa Phi, IEEE, ACM-SIGARCH.